Application Note 202
NV SRAM Frequently Asked Questions

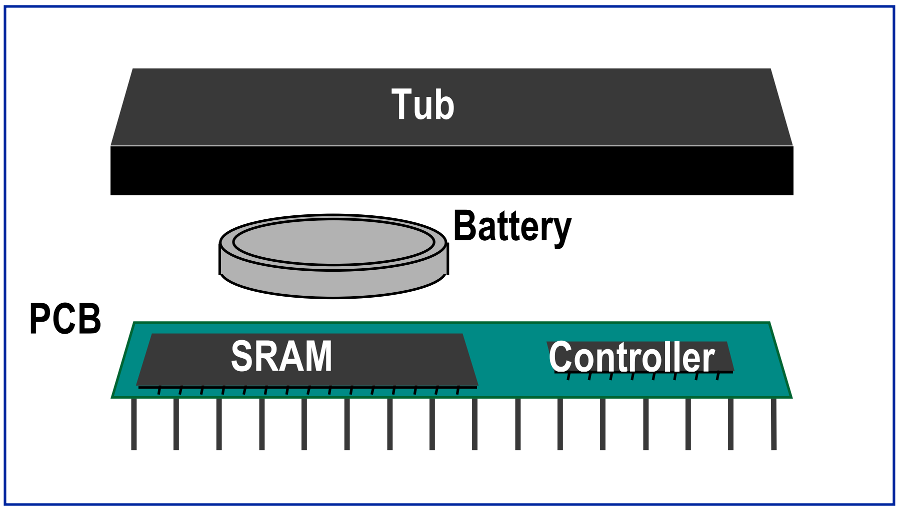
www.maxim-ic.com

What is an NV SRAM?

A nonvolatile static random access memory (NV SRAM) is a type of computer memory that maintains its memory data when power is shut off. NV SRAMs store digital information like system configuration or temporarily store transient digital data, such as what passes through a telecom router, so that it can be recovered in case of a power failure.

An NV SRAM is a nonvolatile memory module built using a standard SRAM, an integrated circuit (IC) controller with a battery switchover circuit, and a lithium battery. All of these components are mounted on a circuit board and encapsulated in a plastic tub. The example below (Figure 1) is pinned out to match the footprint and pinout of a JEDEC standard SRAM so that the two can be used interchangeably.

JEDEC STANDARD SRAM Figure 1

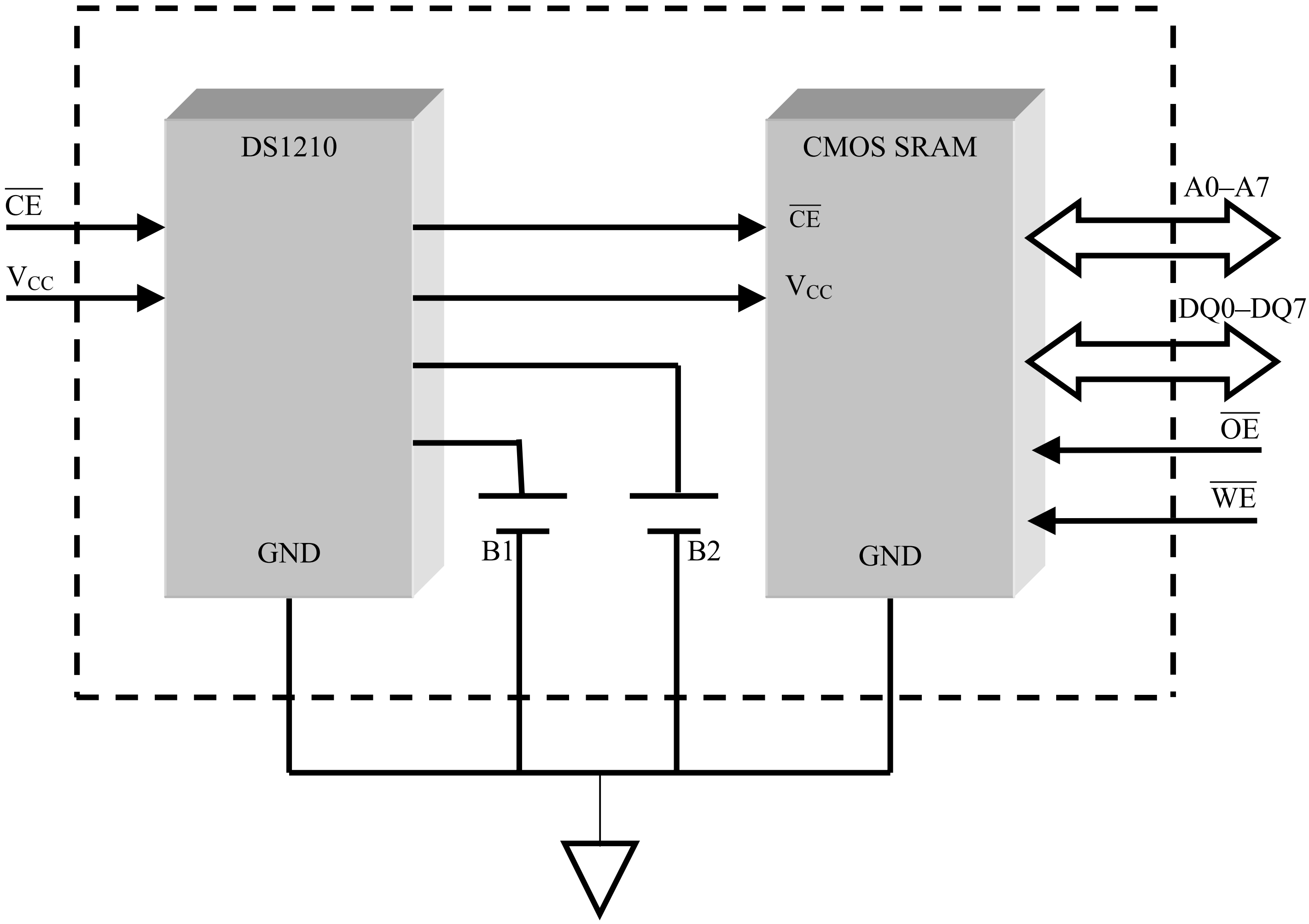


A typical NV SRAM consists of a DS1210 (or similar) nonvolatile controller chip, a lithium coin-cell battery, and a screened, low-standby current SRAM. The DS1210 used in this example is identical to the MXD1210. The controller, in conjunction with the battery, converts the CMOS SRAM into nonvolatile memory.

The DS1210 controller performs two functions. First, it switches between V_{CC} and the lithium battery, depending on the power situation. It also gates the chip-enable signal used to enable the SRAM, allowing access to the SRAM during conditions of good power and inhibiting access to the SRAM during conditions of power-up or power-down.

The DS1210 monitors power for an out-of-tolerance condition. When such a condition is detected, $\overline{CE}$ is inhibited to the SRAM, which write-protects the device as the circuit powers down. At the point when V_{CC} is at the same level as the internal battery voltage, the controller switches SRAM over to one of the two batteries that has the highest voltage and fullest charge. This maintains the memory contents in the SRAM until the next power-up. During power-up, $\overline{CE}$ is maintained high (SRAM inactive) until power is stable for 125ms (max). After that, the NV SRAM can be accessed as if it were a normal SRAM part.

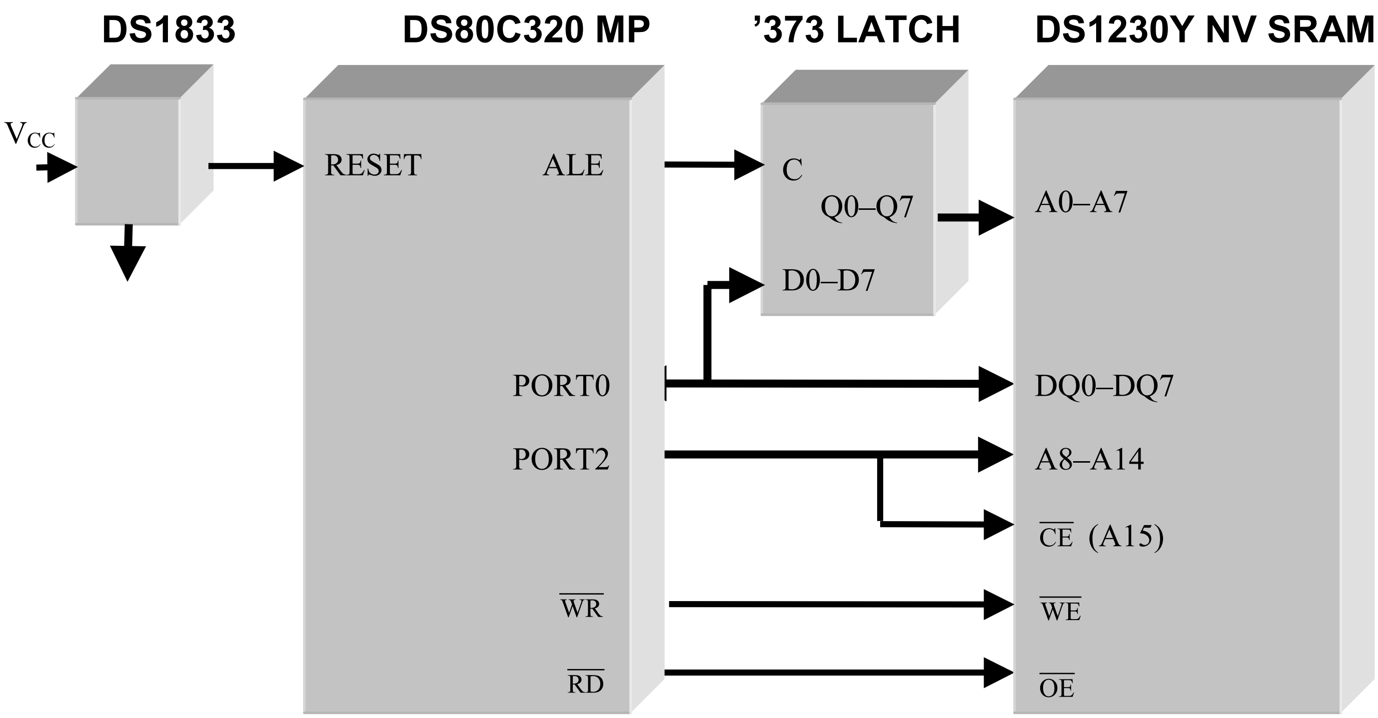
NV SRAM BLOCK DIAGRAM Figure 2



How do I interface to an NV SRAM?

The two most common types of NV SRAMs application interfaces are shown below with the DS80C320 and HC68000 examples. The 8051 has a multiplexed address/data bus that must be demultiplexed before applied to the NV SRAM. The HC68000 uses a demultiplexed bus, but has different control pins and bus timing for performing memory accesses. The NV SRAMs are designed to be compatible with both types of bus architecture, but need to be configured correctly.

NV SRAM Interfaced to DS80C320 Figure 3



In a typical DS80C320 to SRAM application, the designer often uses a configuration very similar to that in Figure 3, with the exception that $\overline{CE}$ is permanently tied low. This works quite well with an SRAM, but $\overline{CE}$ should not be tied low when using an NV SRAM.

A mechanism in the DS1210 controller ensures that the last $\overline{CE}$ is gated through to the SRAM and returns high before actively forcing it high. This prevents partial writes and potential data corruption during the power-down cycle. If $\overline{CE}$ is tied low, however, the controller waits until the battery switch-over time to disable the SRAM. This happens at a much lower voltage than normal.

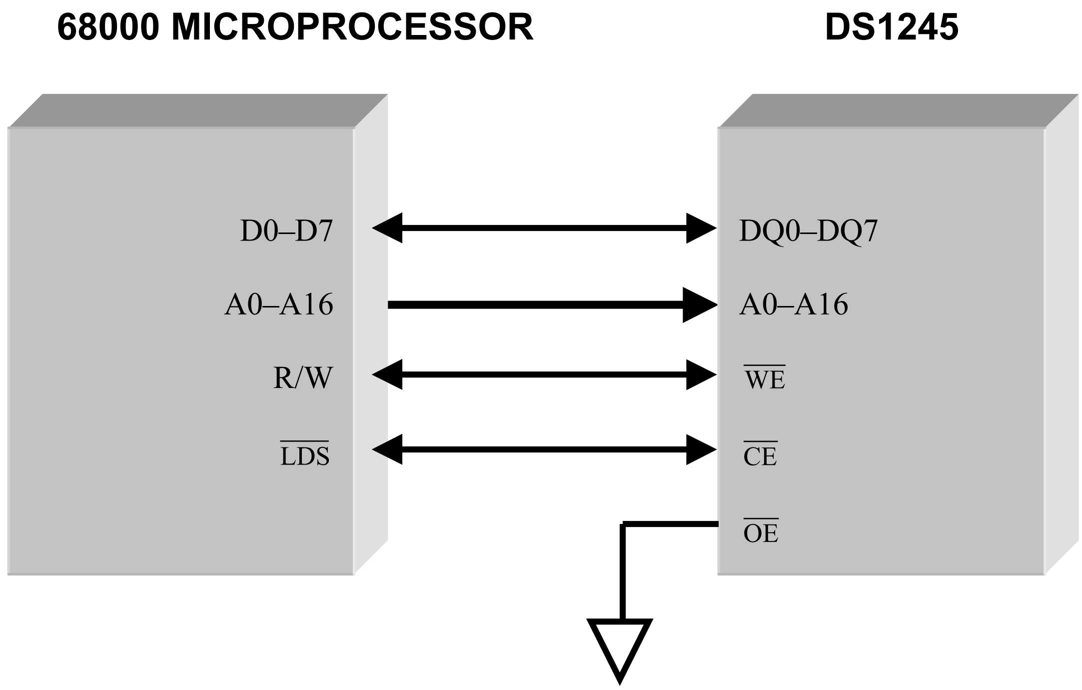
During power-down, decaying power on the address, data, and control lines can be interpreted as random bits. With $\overline{CE}$ tied low, the conditions can be met so that this random data is interpreted as a write cycle, corrupting the memory.

In Figure 3, a CPU supervisor resets the microcontroller at a 5% level, forcing $\overline{CE}$ high and ensuring that $\overline{CE}$ remains high for the reset of the power-down cycle.

Note: Application Note 57 contains information on latch selection as well as memory access requirements for the DS80C320 operating at various speeds.

Interconnect for the MC68000 family of microprocessors is shown in Figure 4. In general, this interconnect works for other Motorola microprocessors.

NV SRAM Interfaced to 68000 Figure 4



Can you turn the freshness seal back on once power has been applied?

(Most NV SRAMS have a freshness seal that isolates the battery from the NV SRAM until it first powers up. This extends the NV SRAM battery's shelf life by removing the SRAM load from the battery until it is installed in the customer's equipment and power cycled.)

No. Controlling the freshness seal requires specialized test equipment that the end user does not have.

The only exception to the rule is the PowerCap™. Resetting the freshness seal is accomplished by removing the DS9034 cap, waiting sufficient time for the controller to bleed down internally (approximately 30 seconds), and then installing a new cap (reusing an old cap is not recommended).

PowerCap is a trademark of Dallas Semiconductor.

Can you measure the voltage of an NV SRAM?

With the exception of PowerCaps with exposed battery contacts, it is not possible to directly measure the voltage of the NV SRAM battery voltage.

Since flash memory is a lot cheaper, why not use it instead of NV SRAM?

When high-speed, read/write capability is needed (as in digital communication equipment), NV SRAM is the only choice. Flash can be read quickly, but generally takes a long time to write. Also, NV SRAM is the only solution if unlimited write cycles are needed. Flash, as well as other memory types, have wear-out mechanisms that limit the number of write cycles. Flash also is limited to block writes, while NV SRAM allows reading and writing to individual bytes of memory.

What replacement parts should I use for the DS16XX line of NV SRAMs since they are obsolete?

The DS16XX line of NV SRAMS were identical in function, package, and pinout to the DS12XX series of NV SRAMs, with the exception that they had the addition capability to write-protect individual blocks of memory. A few years ago they became obsolete but had no replacement. The equivalent DS12XX NV SRAM will work in the socket. The write-protect function, however, is not available.

Why is the battery in my DS1213 SmartSocket going dead?

(The SmartSocket is a socket for standard SRAMs that contain the controller and battery found in NV SRAM. When used with an SRAM, it is functionally identical to a NV SRAM.)

There are two common causes of this problem. First, most water-based circuit board washes, even those using de-ionized water, can leave conductive metal traces plated on the internal circuit board between the terminals of the battery. This puts an excessive load on the battery draining it. A few years back, before the EPA outlawed non-water-cleaning solvents, this was not a problem. The most effective solution is to replace the socket memory with a comparable NV SRAM. A conversion chart is shown in Table 1. Keep in mind that the NV SRAM cannot be plugged into an existing SmartSocket. The battery switchover controller in the SmartSocket will interfere with the operation of the controller in the NV SRAM, causing it to malfunction.

Second, when using a SmartSocket, it is the customer's responsibility to procure SRAM that has a maximum (not typical) standby current of less than 1µA. This will give the SmartSocket an estimated lifetime of 10 years, given the capacity of the batteries we internally use. The customer can save the problem of procuring low-current SRAM, which can be hard to find, by using a comparable NV SRAM. The customer not only eliminates the SRAM but also eliminates problems caused by the water-washing method mentioned earlier. This also eliminates shortened battery lifetimes caused by discharge during operation in high humidity environments. Table 1 has a conversion chart from SmartSockets to NV SRAMS.

SmartSockets to NV SRAM Cross Reference Table 1

SmartSocket	Density SRAM	No. of Pins	NV SRAM
DS1213B	2k x 8k	24	DS1220AB
DS1213B	8k x 8k	28	DS1225AB
DS1213C	32k x 8k	28	DS1230AB
DS1213D	32k x 8k	28	DS1230AB
DS1213D	128k x 8k	32	DS1245AB

I replaced my standard SRAM with an NV SRAM and now my system doesn't work at all. What caused this?

In general, this is caused by one of two things:

First, the designer did not consider the recovery time, or t_{REC}, of the particular NV SRAM selected. On power-up, an internal power monitor disables the NV SRAM until a power-good situation and then holds it disabled for an additional 2ms (max) or 125ms (max), depending on the NV SRAM after power-good. If the microcontroller attempts to access the memory before t_{REC} times out, it will not be able to access the device's memory to read or write, so the system fails. Either a software loop on power-up to extend the access time past t_{REC}, or moving the NV SRAM access somewhere later in the power-on initialization sequence in the microcontroller's firmware will resolve the problem. This problem often can be corrected be selecting a CPU supervisor that has a reset time longer than the recovery time of the NV SRAM.

Second, selecting the voltage levels at which the NV SRAM and the microcontroller become active are critical. If the microcontroller becomes active below 4.5V and the NV SRAM becomes active above 4.75V, the same problem of the microcontroller trying to access a disabled NV SRAM occurs. The power-good threshold for the two devices should force the system to enable the NV SRAM first and then the processor. This involves selecting the NV SRAM with the appropriate power-good level and pairing that with a CPU supervisor that enables the processor at a higher voltage.

The most recent generation of NV SRAMS has a $\overline{\text{RESET}}$ output that is synchronous with its own internal reset. If this is used to reset the microcontroller, the possibility of trying to access a disabled NV SRAM is removed.

Why am I getting data corruption in my NV SRAM?

The most common cause of corruption is electrical. Negative voltage spikes of greater than the specified -0.5V on any input pin, especially when powered down, can cause data corruption. ESD protection diodes on the I/O cause the internal V_{CC} to drop lower than the data-retention level, thus causing data loss. The only way to prevent this from happening is to determine and eliminate the cause of the negative voltage spikes. The same is true for the power input. Some older linear regulators, when configured with a large output decoupling cap, have outputs that go negative when going through power cycles.

Voltages applied to the I/O of the NV SRAM when powered down can cause the NV SRAM to remain inactive when powered up. These voltages on the unpowered part turn on the ESD protection diodes as well, which puts a charge on the internal V_{CC} substrate that is greater than the battery voltage. The switchover from battery to external V_{CC} occurs when the external V_{CC} is greater. If they are the same level, the switchover never occurs and the NV SRAM remains in the shutdown mode. The only way to resolve this is to correct the design so that no I/O pins are active when the device is powered down.

What’s a DS1235?

A number of years ago, Dallas Semiconductor had a product called the DS1235. It was functionally and physically identical to the DS1230, with the exception that it had a five-year data-retention specification instead of 10 years. An alternative is the DS1230 with the same postfix and speed grade (e.g., DS1235Y-150 would be DS1230Y-150).

Are 3.3V parts available?

Yes. We have devices ranging from 256kb to 16Mb. Throughhole and surface mount parts are available. 3.3V devices are indicated by a “W” in the postfix. For a selection guide for these and other NV SRAMs visit the link below:

http://para.maxim-ic.com/compare.asp?Fam=Memory&Tree=Memory&HP=Memory.cfm

Are Dallas NV SRAMs UL recognized?

Yes. Conditions of acceptability for all modules can be found at the link below:

http://www.maxim-ic.com/TechSupport/QA/module.htm

What other functions are available on NV SRAMs?

The DS13**-series of NV SRAMs (DS1330, DS1345, DS1350) have a power-on reset output that can be used to sequence the control of the NV SRAM and the processor during power-up and power-down cycles.

Are any NV SRAMs not recommended for future designs?

Yes. The DS1220Y and DS1225Y are not recommended for new designs. These older devices used a battery reference to determine the power-valid trip-point during power cycles. Newer designs use a bandgap reference. The battery-referenced devices had a trip-point that decreased during the life of the device. Devices using the bandgap had a trip-point that was stable for the life of the product.

The DS1220AD and DS1225AD are recommended for new designs needing the functionality of the DS1220Y and DS1225Y. For existing designs, the DS1220AD or DS1225AD should be considered as replacements. One precaution, however, as the "Y" parts had a reset timeout on the order of milliseconds while the "AD" parts have a timeout of 125ms. When replacing the Y part with the AD part in existing designs, it must be determined that the controlling processor does not become active during a power-up cycle for at least 125ms to ensure that the NV SRAM is active before the processor attempts a memory access.